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A Unique Approach To Develop A Band Gap Reference Voltage Chip

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Abstract-A unique approach to design a Bandgap Reference voltage chip is implemented in 0.25µm CMOS technology. This chip can be designed by using a layout tool microwind 3.1.7 version. Here the simulations is based on tanner tool. The chip circuit generates a reference voltage of 1.23 V . It can operate between 20ºC & 70º C temperature . The parasitic BJI of CMOS process is used in the band gap core. Band gap core produces a voltage that is in sensitive to variation in temperature . This is achieved by summing a positive TC voltage and negative TC voltage. This circuit works in a current feedback mode, and it generates its own reference current, resulting in a stable operation. This bandgap reference circuit can support a zero current even when the power supply is on. Therefore a simple start up circuit is required for successful operation of the system. It has a unique protection with respect to ESD and LATCHUP. The bandgap reference circuit is to design in CMOS process . This helps to avoid BICMOS process which is little bit complicated and much more expensive than CMOS process.

***Keywords*— Bandgap Reference, CMOS, Temperature Independence, ESD,LATCHUP**

I. INTRODUCTION

In recent years, as the rapid development of modern communication and consumer products such like web servers, cellular phones and various PDA products, high quality power supplies that provides them suitable power are in great demand. As results, the research on power management ICs has become a new hot spot for IC designers. And voltage reference, as one of the key modules in power management ICs, is responsible for offering a precision reference voltage to other internal blocks such as regulator, comparators, error amplifiers, DAC (Digital Analog Converter), OSC (Oscillator) and etc. Sometimes, it also offers external reference voltage through an additional pin.

Target: A fixed dc reference voltage that does not change with temperature.

Fig1:Block diagram of bandgap reference circuit

As a well-established reference generator technique, bandgap reference is most popular for both Bipolar and CMOS technologies. The principle of the bandgap circuits relies on two groups of diode-connected BJT transistors running at different emitter current densities. By canceling the negative temperature dependence of the PN junctions in one group of transistors with the positive temperature dependence from a PTAT (proportional-to-absolute-temperature) circuit which includes the other group of transistors, a fixed DC voltage which doesn't change with temperature is generated. This voltage is typically 1.23 volts, which is approximately the band gap of silicon. .

II. CIRCUIT DESCRIPTION

A reference voltage is generated by adding two voltages that have temperature coefficients of opposite sign with suitable multiplication constants. The resulting voltage obtained is independent of temperature. The diode voltage drop across the base-emitter junction, VBE, of a Bipolar Junction Transistor (BJT) changes Complementary to Absolute Temperature (CTAT) [1]. Whereas if two BJTs operate with unequal current densities, then the difference in the base emitter voltages, ΔVBE, of the transistors is found to be Proportional to Absolute Temperature (PTAT). The PTAT relationship is given by [2],

Eq1…… $$\Delta V_{BE} = V_T \ln m; \quad V_T = kT / q$$

where, k is Boltzmann's constant, T is the absolute temperature, q is the electron charge and m is the ratio of the current densities of the two BJTs. The PTAT voltage may be added to the CTAT voltage with suitable weighting constants to obtain a constant reference voltage

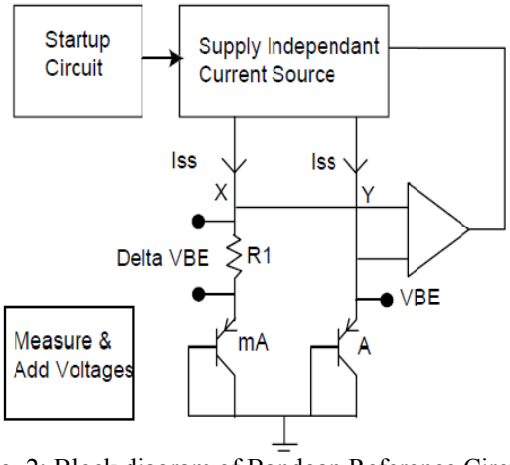


Fig. 2: Block diagram of Bandgap Reference Circuit.

Figure 2 shows the block diagram of the bandgap reference circuit designed. By using a supply independent current source, a current ISS is passed through BJT A. The same current ISS flows through m transistors connected in parallel, identical to A. Thus the current density of A is m times the current density of the m BJTs identical to A, connected in parallel. The voltages at node X and Y are maintained at the same value, VBE using a feedback network through a differential amplifier. This results in a

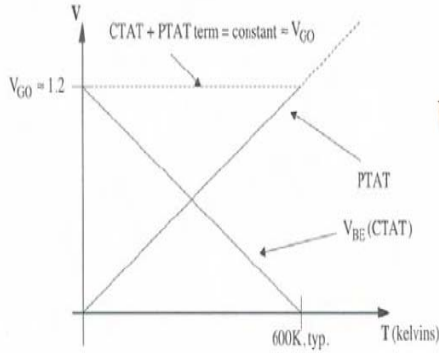
voltage of ΔVBE, across the resistor R. The voltages VBE and ΔVBE are added to obtain the reference voltage. The circuit also requires a startup circuit since there exists a stable state at which no current flows through the circuit. The startup circuit forces the transistors to turn on and the circuit to operate at its other stable state to generate the reference voltage.

Eq2

$$Vref = V_{BE} + \Delta V_{BE} \cdot \frac{R1}{R2}$$

R2 the weighting constant

Thus by selecting the value of R2 the weighting constant may be set. This arrangement provided an elegant arrangement to generate the reference voltage while conserving voltage headroom. The circuit has a stable operating point at which no current to flows through it. An arrangement must be made to force the saturation when the supply is turned on. This function is carried out by the startup circuit. Thus output voltage is actually summation of a positive TC and a negative TC voltage. By choosing the proper value of resistors, output reference voltage is made constant with respect to temperatures (Zero TC).



$$V_{BE} + M\frac{kT}{q} \cong V_{G0} - \frac{kT}{q} ln\left(\frac{I_0}{I_C}\right) + M\frac{kT}{q}$$

$$\cong V_{G0} + \frac{kT}{q}\left(M - ln\left(\frac{I_0}{I_C}\right)\right)$$

Combining VBE and an appropriately scaled version of kT/q produces a temperature independent voltage, equal to VG0

A. Startup Circuit

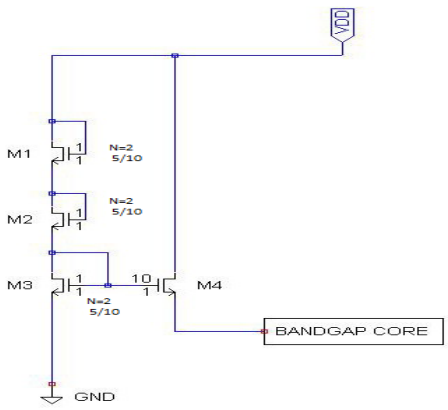


Fig. 3 Startup circuit

In the circuit of bandgap core, if all of the transistors carry zero current when the supply is turned on, they may remain off indefinitely because the loop can support a zero current in both branches. So it is needed to inject current in the bandgap core for proper operation of the circuit. Start up circuit does this job. This circuit also turns off when steady state is reached. A very simple start up circuit is used in this bandgap circuit.

B. *pnp* BJT using CMOS process

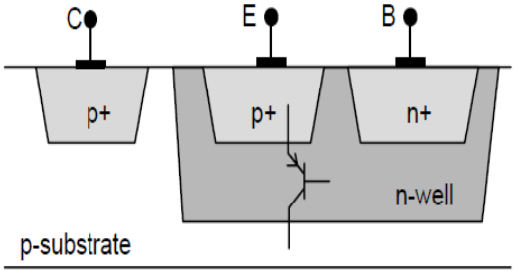
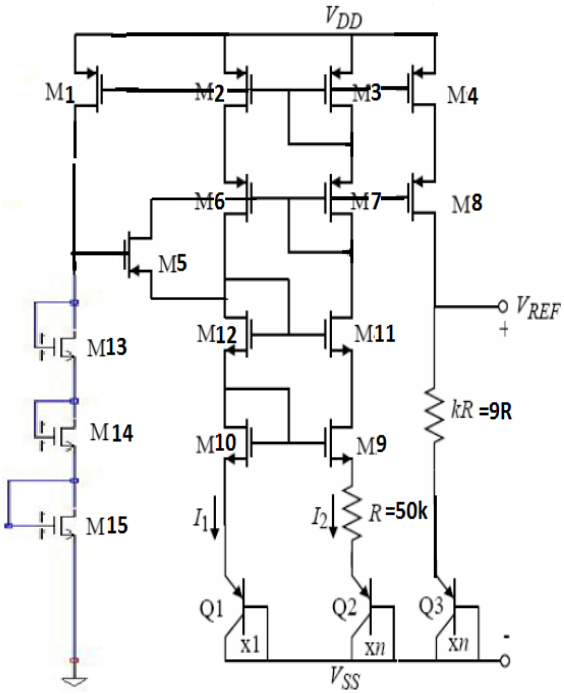


Fig. 4: *pnp* BJT using CMOS process

It should be noted that an ideal BJT is not available in CMOS technology. A *pnp* BJT is made using the n-well normally associated with a PFET [1] (Figure 4), the p substrate behaving as the collector.

III.. SCHEMATIC OF COMPLETE CIRCUIT



A.Layout for the BGR in 0.25µm CMOS technology using microwind tool

- The package contains a library of common logic and analog ICs to view and simulate.
- MICROWIND3includes all the commands for a mask editor as well as original tools never gathered before in a single module2D and 3D process view, Verilog compiler, tutorial on MOS devices).

- The MICROWIND3 allows the student to design and simulate an integrated circuit at physical description level.
- You can gain access to Circuit Simulation by pressing one single key.

IV. SIMULATION RESULTS

The bandgap reference voltage gives a voltage of 1.23 V when adjusted to have a zero temperature coefficient at 27C based on the tanner v12.6. Figure 2, shows the result of the simulation. It can be adjusted to give a voltage of 1.26V, by sacrificing the zero temperature coefficient at 27C, but this leads to a much more degraded response. Figure 5, shows the result of the transient simulation.

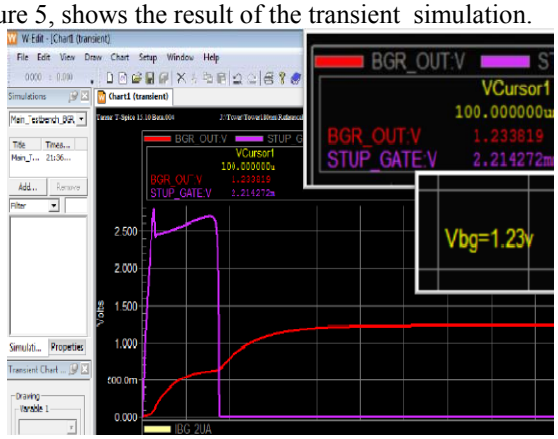


Fig 5.Transient simulation with startup

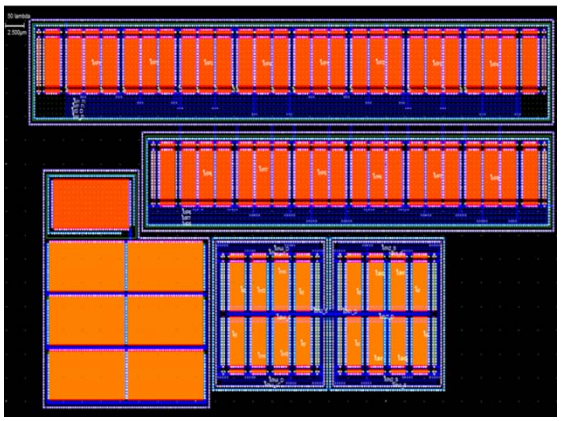


Fig 6

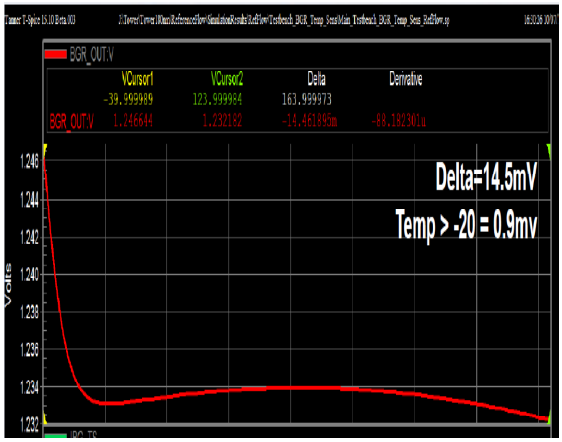


Fig 7 .Temprature sensitivity

Figure 8 shows the a.c response. A PSRR of 59dB is obtainedat d.c at the high frequency corner of 10Mhz, the PSRR startsto degrade ans is about 10dB for a frequency of abou 20Mhz.This problem can be solved by putting a 100pF capacitorbetween Vdd and ground to suppress the noise in Vdd. Thiswould probably be done external to the chip as it is not feasible to put the supply bypass capacitor on-chip.

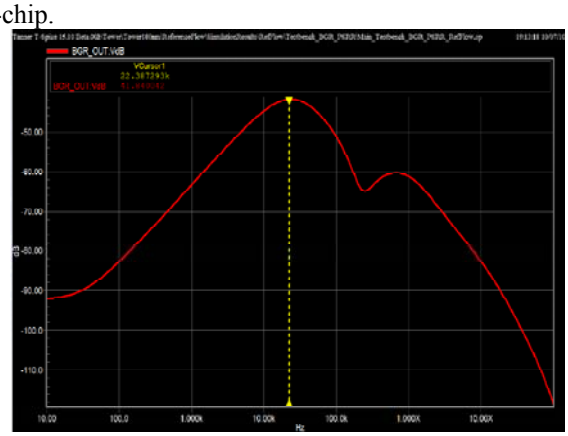


Figure 8 3.PSRR

CONCLUSION

A bandgap reference with a current feedback mode hasbeen designed. The circuit uses no external current sourcesand is designed to have a zero temperature coefficient at 27C.The design is implemented with 0.25µm CMOS process and consumes very little headroom .The chip occupies a total area of the chip has been optimized by combining all the MOSs. Most of the area is taken up by the pnp transistors, so it cannot be optimized too much.The bandgap reference circuit can support a zero current even when the power supply is on. So for proper operation the circuit needs to be turned on.This helps to avoid BiCMOS process which is a little bit complicated and much more expensive than CMOS process. A fixed dc reference voltage that does not change with temperature. Useful in circuits that require a stable reference voltage circuits like ADC .

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